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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,221	09/20/2006	Hajime Nagai	JP03 0006 US1	5690

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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

EXAMINER	
TRAN, THIENVU V	
ART UNIT	PAPER NUMBER
2819	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/566,221	NAGAI, HAJIME	
	Examiner	Art Unit	
	Thienvu V. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *20 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) *12-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/26/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because **Figures 1 and 2** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. **Claims 1-11** are rejected under 35 U.S.C. 102(a) as being anticipated by the Applicant's own admitted prior art.

Regarding claim 1, Applicant's admitted prior art teaches a device (100) (fig. 1) comprising:

a first input portion (In1) (fig. 1) for receiving a first input signal (SI1) (fig. 1);

a first output portion (So1) (fig. 1) for outputting a first output signal (Out1) (fig. 1); and

a first voltage dropping means (2) (fig. 1) for dropping a voltage on a first node (N1) (fig. 1) before changing from a state in which the first input portion is disconnected from the first node (i.e., when transistor 2 is deasserted, the first input portion In1 will be disconnected from node N1) (see fig. 1) to a state in which the first input portion is connected to the first node (i.e., when transistor 2 is asserted, the first input portion In1 will be connected to the first node N1) (see fig. 1), the first node located between the first input portion and the first output portion (i.e., N1 is located between In1 and So1) (see fig. 1).

Regarding claim 2, Applicant's admitted prior art teaches a voltage converting device (100) (fig. 1) for receiving a first input signal (SI1) (fig. 1) having a first high input voltage and a first low input voltage (i.e., from t0-t1, the first input voltage is a high signal, and from t1-t4, the first input voltage is a low signal) (see fig. 2), the first high input voltage having a relatively high voltage level and the first low input voltage having a relatively low voltage level (see fig. 2), wherein the voltage converting device converts at least one of the first high input voltage and the first low input voltage and outputs the first input signal having a converted voltage level as a first output signal (i.e., the first output So1 is converted to a high output voltage, Vo_high)(see fig. 2), wherein the voltage converting device comprises:

a first input portion (In1) (fig. 1) for receiving the first input signal (SI1) (fig. 1);

a first output portion (So1) (fig. 1) for outputting the first output signal (Out1) (fig. 1); and

a voltage converting means (100) (fig. 1) for converting at least one of the first high input voltage and the first low input voltage, and wherein the voltage converting means comprises a first voltage dropping means (2) (fig. 1) for dropping a voltage on a first node (N1) (fig. 1) before changing from a state in which the first input portion is disconnected from the first node (i.e., when transistor 2 is deasserted, the first input portion In1 will be disconnected from node N1) (see fig. 1) to a state in which the first input portion is connected to the first node (i.e., when transistor 2 is asserted, the first input portion In1 will be connected to the first node N1) (see fig. 1), the first node located between the first input portion and the first output portion (i.e., N1 is located between In1 and So1) (see fig. 1).

Regarding claim 3, the Applicant's admitted prior art teaches the voltage converting means comprises first conversion voltage supplying part (21) (fig. 1) for supplying the first node with a first conversion voltage for converting one of the first high input voltage and the first low input voltage (power supply voltage 21 supplies high voltage to the first node) (see fig. 1), the first conversion voltage having a higher voltage level than the first high input voltage (see background, DESCRIPTION OF RELATED ART, lines 25-28), and wherein the first voltage dropping means (2) (fig. 1) drops a voltage on the first node (N1) (fig. 1), before changing from a state in which the first input portion is disconnected from the first

node (i.e., when transistor 2 is deasserted, the first input portion In1 will be disconnected from first node N1) (see fig. 1) and the first conversion voltage supplying part is connected to the first node to a state in which the first input portion is connected to the first node (i.e., when transistor 2 is asserted, the first input portion In1 will be connected to the first node N1) (see fig. 1).

Regarding claim 4, the Applicant's admitted prior art teaches the voltage converting means comprises second conversion voltage supplying part (22) (fig. 1) for supplying the first node with a second conversion voltage (Vs_low=ground) (fig. 1) for converting the other of the first high input voltage and the first low input voltage, the second conversion voltage having a voltage level lower than or equal to the first high input voltage (see background, DESCRIPTION OF RELATED ART, lines 28-29), and wherein the first voltage dropping means (2) (fig. 1) connects the second conversion voltage supplying part instead of the first conversion voltage supplying part to the first node (i.e., first node N1 is connected to ground when the pull-down transistor of inverter 11 is asserted) (fig. 1), before changing from a state in which the first input portion is disconnected from the first node (i.e., when transistor 2 is deasserted, the first input portion will be disconnected from the first node N1) (see fig. 1) and the first conversion voltage supplying part is connected to the first node (i.e., first node N1 is connected to power supply 21 through invert 12) (see fig. 1) to a state in which the first input portion is connected to the first node (i.e., when transistor 2 is asserted, the first input portion will be connected to the first node) (see fig. 1).

Regarding claim 5, the Applicant's admitted prior art teaches the first voltage dropping means comprises:

a first switching means (11) (fig. 1) for making a first connection state in which the second conversion voltage supplying part is connected to the first node (i.e., a first connection state would be when the pull-down transistor of inverter 11 is asserted, the first node will be connected to ground) (see fig. 1) and a first disconnection state in which the second conversion voltage supplying part is disconnected from the first node (i.e., a first disconnection state would be when the pull-down transistor of inverter 11 is deasserted, the first node will not be connected to ground); and

a first driving circuit for driving the first switching means (50) (fig. 1) (e.g., when transistor 2 is asserted, inverter 11 will be driven by signal source 50).

Regarding claim 6, the Applicant's prior art teaches the second conversion voltage has the same voltage level as the first low input voltage (see background, DESCRIPTION OF RELATED ART, lines 28-29).

Regarding claim 7, the Applicant's admitted prior art teaches the voltage converting device receives a second input signal (SI2) (fig. 1) having a second high input voltage and a second low input voltage (i.e., from t0 to t1, the second input is a low signal and from t1 to t4, the second input is a high signal) (see fig. 2), the second high input voltage having a relatively high voltage level and the second low input voltage having a relatively low voltage level (see fig. 2), wherein the voltage converting device converts at least one of the second high input

voltage and the second low input voltage and outputs the second input signal having a converted voltage level as a second output signal (see second output, So2, of fig. 2).

Regarding claim 8, the Applicant's admitted prior art teaches the voltage converting device comprises second input portion (In2) (fig. 1) for receiving the second input signal (SI2) (fig. 1) and second output portion (So2) (fig. 1) for outputting the output signal (Out2) (fig. 1), and wherein the voltage converting means comprises a second voltage dropping means (3) (fig. 1) for dropping a voltage on a second node (N2) (fig. 1) before changing from a state in which the second input portion is disconnected from a second node (i.e., when transistor 3 is deasserted, the second portion will be disconnected from the second node N2) (see fig. 1) to a state in which the second input portion is connected to the second node (i.e., when transistor 3 is connected, the second portion In2 will be connected to the second node N2) (see fig. 1), the second node located between the second input portion and the second output portion (i.e., N2 is located between second node In2 and second ouput So2) (see fig. 1).

Regarding claim 9, the Applicant's admitted prior art teaches the voltage converting means comprises first conversion voltage supplying part (21) (fig. 1) for supplying the first node with a first conversion voltage for converting one of the first high input voltage and the first low input voltage (i.e., power supply 21 supplies high voltage to node N1) (see fig. 1), the first conversion voltage having a higher voltage level than the first high input voltage (see background,

DESCRIPTION OF RELATED ART, lines 26-28), and wherein the first voltage dropping means drops a voltage on the first node (i.e., when transistor 2 is asserted, a voltage drop will be at node N1) (see fig. 1), before changing from a state in which the first input portion is disconnected from the first node and the first conversion voltage supplying part is connected to the first node (i.e., when transistor 2 is deasserted, the first input portion will be disconnected from the first node N1 and the power supply 21 will be connected to the first node N1 through inverter 12) (see fig. 1) to a state in which the first input portion is connected to the first node (i.e., when transistor 2 is asserted, the first input portion will be connected to node N1) (see fig. 1).

Regarding claim 10, the Applicant's admitted prior art teaches the voltage converting means comprises second conversion voltage supplying part (22) (fig. 1) for supplying the first node with a second conversion voltage for converting the other of the first high input voltage and the first low input voltage (i.e., the second supplying voltage, ground, is connected to first node N1 through inverter 11) (see fig. 1), the second conversion voltage having a voltage level lower than or equal to the first high input voltage (see background, DESCRIPTION OF RELATED ART, lines 28-29), and wherein the first voltage dropping means connects the second conversion voltage supplying part instead of the first conversion voltage supplying part to the first node (i.e., when transistor 2 is deasserted, the first node N1 is connected to power supply 22, ground, through pull-down transistor in inverter 11) (see fig. 1), before changing from a state in which the first input

portion is disconnected from the first node and the first conversion voltage supplying part is connected to the first node (i.e., when transistor 2 is deasserted, the first input portion will be disconnected from the first node and power supply 21 will be connected to the first node N1 through inverter 12) (see fig. 1) to a state in which the first input portion is connected to the first node (i.e., when transistor 2 is asserted, the first input portion will be connected to first node N1) (see fig. 1).

Regarding claim 11, the Applicant's admitted prior art teaches the voltage converting means comprises third conversion voltage supplying part (21) (fig. 1) for supplying the second node with a third conversion voltage for converting one of the second high input voltage and the second low input voltage (i.e., the second node N2 is connected to power supply 21 through inverter 12) (see fig. 1) the third conversion voltage having a higher voltage level than the second high input voltage (see background, DESCRIPTION OF RELATED ART, lines 26-28), and wherein the second voltage dropping means drops a voltage on the second node (i.e., when transistor 3 is asserted, a voltage drop is at node N2) (see fig. 1), before changing from a state in which the second input portion is disconnected from the second node and the third conversion voltage supplying part is connected to the second node (i.e., when transistor 3 is deasserted, the second input portion will be disconnected from second node N2) (see fig. 1) to a state in which the second input portion is connected to the second node (i.e.,

when transistor 3 is asserted, the second input portion will be connected to node N2) (see fig. 1).

Allowable Subject Matter

4. **Claims 12-19** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 12, the prior art does not fairly teach or suggest the second voltage dropping means connects the fourth conversion voltage supplying part instead of the third conversion voltage supplying part to the second node, before changing from a state in which the second input portion is disconnected from the second node and the third conversion voltage supplying part is connected to the second node to a state in which the second input portion is connected to the second node.

Regarding claims 13-19, they depend on claim 12 above.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thienvu V. Tran whose telephone number is (571) 270-1276. The examiner can normally be reached on Monday-Friday (7:30AM-5:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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T.T/

REXFORD BARNIE
SUPERVISORY PATENT EXAMINER
04/01/07